IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of GERRIT J. KEESMAN

Atty. Docket PHB 33,946C

Serial No. 08/901,338

Group Art Unit: 2613

Filed: July 28, 1997

Examiner: A. RAO

BUFFER MANAGEMENT IN VARIABLE BIT-RATE COMPRESSION SYSTEMS

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPEAL BRIEF

Sir:

This is an appeal from the final rejection of Claims 1-12, and 14.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, U.S. Philips Corporation, a Delaware corporation. The ultimate parent of the assignee is Koninklijke Philips Electronics, N.V., a Dutch corporation.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeal, which is directly related to this case. Appellant is not aware of any related interferences.

III. STATUS OF CLAIMS

Claims 1-12 and 14 stand rejected under 35 USC Section 102.

IV. STATUS OF AMENDMENTS

The Examiner's Advisory Action dated February 14, 2001, indicated that Appellant's response under Rule 116, filed January 31, 2001, was considered by the Examiner, but did not place the application in condition for allowance. No amendment to the specification or the claims was made or entered. A Notice of Appeal was filed on January 31, 2001.

V. SUMMARY OF INVENTION

Appellant's invention pertains to a method and apparatus for the compression of digital video signals. More particularly, Appellant's invention pertains to preventing overflow or underflow of a decoder buffer when a variable bit-rate data channel links encoder and decoder. Appellant's invention provides greater efficiency in encoder buffer management by deriving a second output bit rate of the encoder as a percentage of a first input bit rate to the encoder in order to provide a tunable delay for the encoder. The second bit rate percentage varies inversely with changes in the first bit rate such that the contents of the decoder buffer will remain substantially constant. Figures 3 and 5 are embodiments of the present invention and illustrate the tunable delay.

VI. THE ISSUES

The principal issue is whether the 35 USC § 102 rejection of Claims 1-12 and 14 is correct. More

specifically, the issue is whether the Examiner's interpretation of column 10, lines 15-25 of US Patent No. 5,561,466 to Kiriyama is correct.

VII. GROUPING OF THE CLAIMS

The rejected claims stand or fall together.

VIII. THE ARGUMENT

A. The Examiner's Interpretation of column 10, lines 16-22 of Kiriyama is Incorrect.

The Examiner stated on page 5 of the Office Action of June 30, 1999, and maintained in subsequent Office Actions of November 16, 1999, May 16, 2000, November 11, 2000, and February 14, 2001, that Kiriyama discloses "'...the output bit rate as being inversely related to the input bit rate...' as in the claims". In making this assertion, the Examiner refers to column 10, lines 15-25 of Kiriyama. These lines state:

> "a sum delay of the delay in the buffer memory 39 of FIG. 5 plus the additional video delay becomes equal to a predetermined video delay threshold value THV. In this manner, the read video data are produced from the video buffer memory 71 with the sum delay relative to supply of the encoded video signal to the buffer memory 39 in the data multiplexer device. It is consequently

possible in the data multiplexer device to know the propagation delay".

On page 3 of the Office Action of February 2, 1999, the Examiner explained the basis for his position, stating "What Kiriyama does disclose is that the system and method manipulates the output time in accordance with the detected delay (Kirayama: column 10, lines 15-25). The delay is the encoder delay + the buffer read out delay + THV, where the THV is the allowable delay of the system and is set threshold which is constant. Accordingly, if the encoder delay increases, the buffer read-out delay is made to decrease in order to keep that timing relation fixed. . . Since there is a direct correlation of the with this timing manipulation to the 'bit-rates', the Examiner maintains that the process sufficiently reads on the recited 'determining the output bit rate as a percentage of the read in bit rate...' as in the instant invention."

Appellant respectfully submits that this is a mischaracterization of Kiriyama. Appellant submits that in Kiriyama, the bit rate of the data stream leaving the decoder buffer (B2) must be equal to the encoder buffer input rate (B1), a constant time later, and need only satisfy a synchrony time delay constant (THV). As stated in lines 16-19 of column 10 of Kiriyama: "A sum delay of the delay in the buffer memory 39 [of the encoder/multiplexer]

plus the additional video delay becomes equal to the predetermined video delay threshold value THV". Therefore, the constant delay criteria in Kiriyama does not define any relationship between B1, (the input bit rate to the encoder buffer) and B2, (encoder buffer output rate). B2 in Kiriyama is only a function of the output data signal exit time from the decoder (THV).

Kiriyama is not a buffer control invention and solves a different problem than the current invention. Kiriyama specifies this constant delay so that lip synchronism can be achieved, i.e. the audio and video will correspond. Appellant's figure 3 explains why the relationship between B1 and B2 is not specified by the constant delay criteria in Kiriyama. In the figure, the encoder buffer input rate B1 is denoted as p[n]. In the present invention, B2 is not represented by p[n-d], the delayed decoder buffer output rate. B2 is represented by R[n], i.e., a second bit rate as a percentage of the first bit rate, which percentage changes inversely in relation to changes in the first bit rate, as claimed in independent Claims 1, 5, and 12. In the present invention, the second bit rate (B2) is generated so that the decoder buffer has a content which has a "substantially constant fullness level . . . in response to changes in the detected current bit rate", as claimed in Claim 12. In the present invention, B2 represents the rate at which the encoded digital video bit stream is read out of the encoder

buffer. B2 is generated without regard to the output rate from the decoder.

B2, as derived in the present invention, is not necessarily equal to the decoder output rate, what the Examiner refers to as B2 in Kiriyama, because in Kiriyama, the decoder buffer adds the delay necessary to achieve synchrony between the audio and the video (THV). What the Examiner refers to as B2 in Kiriyama is not the same B2 as in the current invention and is not derived in the same manner. B2 in Kiriyama is only a function of the output data signal exit time from the decoder (THV) and therefore does not "change inversely in relation to changes in the first bit rate in order to transmit the output data signal to a decoder buffer at the second bit rate" as claimed in the present invention.

B. The Examiner's Argument is Flawed Because His Statement that "the delay is based on a 'sum delay of the delay in the buffer memory 39 of Fig. 5 plus additional video delay becomes equal to a predetermined video delay threshold value THV'" is an Inaccurate Quotation of Kiriyama and Interpreted Out of Context.

The Examiner's rejection of claims 1-12 and 14, in the Office Action of November 1, 2000 is based upon his interpretation of the above lines in Kiriyama, viz. column 10, lines 15-25, already cited above in this Appeal. Appellant respectfully submits that 1) these lines are

misquoted by the Examiner and 2) these lines must be read in conjunction with column 9 lines 59-62 of the Kiriyama specification.

Firstly, the correct quotation of lines column 10, lines 15-25 is as follows:

> "a sum delay of the delay in the buffer memory 39 of FIG. 5 plus **the** additional video delay becomes equal to a predetermined video delay threshold value THV." (emphasis added)

"The additional video delay" has already been defined at column 9, lines 59-62, as follows.

> "**From the video buffer memory 71**, the read video data are read with **an additional video delay** relative to production of the separated video data from the video processor 65".

Based on the above lines, Appellant respectfully disagrees with the Examiner regarding the meaning of the phrase, "additional video delay."

The Examiner states on page 2 of the Office Action that column 9, lines 63-68 and column 10, lines 1-42 "establishes the fact the delay is based on 'a sum delay of the delay in the buffer memory 39 of Fig. 5 plus additional video delay becomes equal to a predetermined video delay threshold value

THV...' and further discloses that the 'sum delay relative to the supply of the encoded video signal to the buffer memory 39 in the multiplexer device...' can be used to find the 'propagation delay...' of the multiplexer device . . . establishes the fact that 'sum delay' doesn't not include or account for the decoder buffer delay as the Applicant asserts . . . but only accounts for elements in codec chain between the encoder and the decoder buffer input."

Appellant respectfully submits that "additional video delay" is applied reading "from the video buffer memory 71" (decoder), as the Kiriyama specification discloses, not writing into this memory. Accordingly it cannot be the case that the additional video delay only accounts for elements in the code chain between the encoder and the decoder buffer input as the Examiner asserts. In Kiriyama, it is the decoder buffer output rate which is relevant as it determines, along with the decoder buffer input rate, the additional video delay. This is not the case in the present invention, wherein B1 and B2 are calculated in order to "transmit the output data signal to a decoder buffer at the second bit rate".

Additionally, in Kiriyama, the encoder buffer 39 is described at column 6, lines 35-36 as "[r]esponsive to the video read control signal", which is "produced by [the] buffer read controller 47" and is a function of "the buffer occupancy signal" and also the "cell or clock control signal

CLCNT", column 6, lines 47-49. As the buffer is responsive to the video read control signal, the buffer read out rate must also be a function of the buffer occupancy signal and the CLCNT signal. There is no mention of the encoder buffer 39 readout rate having an inverse relationship with the very same encoder's buffer 39 read-in rate. Rather, the relationship disclosed in Kiriyama is between the input of encoder buffer 39 and the output of video buffer memory 71.

In summary, the recitation in independent claim 1, and similar recitations in independent claims 5 and 12 of deriving "a second bit rate as a percentage of the first bit rate, which percentage changes inversely in relation to changes in the first bit rate in order to transmit the output data signal to a decoder buffer at the second bit rate" is no where taught or suggested in Kiriyama. Therefore, Applicant respectfully submits that Kiriyama is not prior art to the present invention.

IX. CONCLUSION

Appellant respectfully submits that Appellant has answered each issue raised by the Examiner and that the application is accordingly in condition for allowance. Such allowance is therefore respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

It is hereby certified that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to:

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On March 30 2001

By

APPENDIX

1. (seven times amended) A method of compression for transmission of encoded digital video signals having a variable number of data bits per image frame, comprising the steps of:

a) detecting a first bit rate of an encoded digital video signal bit stream;

b) sequentially writing the encoded digital video signal bit stream in an encoder buffer at the first bit rate;

c) deriving a second bit rate as a percentage of the first bit rate, which percentage changes inversely in relation to changes in the first bit rate; and

d) reading the encoded digital video bit stream out of the encoder buffer at the second bit rate; and transmitting the encoded digital video bit stream to a decoder buffer at the second bit rate.

2. (amended) A method as claimed in Claim 1, wherein for a specified range of first bit rates, the second bit rate equals the minimum first bit rate in said range.

3. (three times amended) A method as claimed in Claim 1, wherein successive groupings of one or more image frames are specified, and the second bit rate is derived from a bit rate of the first frame of the grouping and maintained

constant until the bit rate of a first frame of a succeeding grouping is detected.

4. (amended) A method as claimed in Claim 3, wherein for signals encoded according to the MPEG standard, a first grouping is assigned to I-pictures and a second grouping is assigned to other types of images.

5. (seven times amended) A video signal encoding apparatus for encoding a received digital video signal for transmission, the apparatus comprising:

an encoder stage for encoding a received video signal according to a predetermined coding algorithm and producing the encoded video signal as a variable bit-rate data stream at an output of said encoder stage;

a buffer coupled to receive said variable bit-rate data stream from the encoder stage and arranged to output a data signal corresponding thereto for transmission; and

means coupled to said encoder stage to (i) detect the bit-rate of said variable bit-rate data stream, (ii) derive a second bit rate as a percentage of the detected bit-rate, which percentage changes in inverse relation to changes in the detected bit rate, (iii) control said buffer to produce said output data signal at second bit rate, and (iv) transmit the output data signal to a decoder buffer at the second bit rate; wherein the detected bit rate and said second bit rate are variable.

6. Apparatus according to Claim 5, wherein the encoder stage is configured to encode the received video signal in accordance with the MPEG standard.

7. (twice amended) Apparatus according to Claim 5, wherein said means for detecting a bit rate stores a plurality of contiguous ranges of bit rate values and, on first detecting an encoder output bit rate falling within a first of said ranges, maintains the derived second bit rate substantially constant until a detected encoder output bit rate falls with another of said ranges.

8. (twice amended) A method as claimed in Claim 1, wherein an instantaneous bit rate of an image frame of the encoded digital video signal bit stream is inversely related to a bit density of an image frame of said bit stream n frame periods later, where n is determined by said bit density.

9. (three times amended) A method as claimed in Claim 2, wherein successive groupings of one or more image frames are specified, and the second bit rate is derived from a bit rate of the first frame of the grouping and maintained constant until the bit rate of a first frame of a succeeding grouping is detected.

10. The method as claimed in Claim 1, wherein the step of deriving the second bit rate is carried out by changing the percentage of the first bit rate in response to changes in the first bit rate in such a manner as to maintain a substantially constant fullness level of the buffer.

11. The apparatus as claimed in Claim 5, wherein the means coupled to said encoder stage derives the second bit rate by changing the percentage of the first bit rate in response to changes in the first bit rate in such a manner as to maintain a substantially constant fullness level of said buffer.

12. (amended) A method of compression for transmission of an encoded digital bit stream having a variable bit rate, comprising the steps of:

detecting a current bit rate of the encoded digital bit stream;

sequentially writing the encoded digital bit stream into a buffer at the detected current bit rate;

reading the encoded digital bit stream out of the buffer at a buffer read bit rate; and,

varying the buffer read bit rate in such a manner as to maintain a substantially constant fullness level of the buffer in response to changes in the detected current bit rate, wherein the buffer read bit rate is a percentage of the detected current bit rate, which percentage varies

inversely in relation to changes in the detected current bit rate.

14. The method as set forth in Claim 12, wherein a delay between the input and output of the buffer varies as a function of the detected current bit rate, so that the delay is relatively higher for a detected current bit rate which is higher than a prescribed bit rate and is relatively lower for a detected current bit rate which is lower than the prescribed bit rate.